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Appl. No. 10/603,361

Reply to Office Action of 12/12/2006
Response dated 02/12/2007

FEB 12 2007

Attorney Docket No.: N1085-00089
TSMC 2002-0917**REMARKS/ARGUMENTS**

Claims 1-18 are pending in the subject application and each of claims 1-18 has been rejected. No claim amendments are being filed herein. Applicants respectfully request re-examination, reconsideration and allowance of each of pending claims 1-18.

I. Rejection of Claims 1, 3-5, 9, 14-15 and 18

In paragraph 2 of the Office action, claims 1, 3-5, 9, 14-15 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark, et al. (USPN 6,767,793), hereinafter "Clark" in view of Inaba, et al. (USPN 6,525,403), hereinafter "Inaba." Applicants respectfully submit that these claim rejections are overcome for reasons set forth below. Claim 1 stands as the independent claim of the rejected claim set.

Independent claim 1 is a method claim that recites the features of:

coating a layer of gate electrode material over top and past the opposed sides of a semiconductor device; and

planarizing the layer of gate electrode material to produce a substantially planar surface formed only of the gate electrode material disposed atop the semiconductor device and extending distally past each of the opposed sides, prior to patterning the gate electrode material to form a discrete multiple gate electrode on the semiconductor device, the substantially planar surface having the same height at locations superjacent the semiconductor device and at locations distal the semiconductor device.

Claim 1 clearly provides the feature of planarizing the layer of gate electrode material prior to patterning it. It is because of this sequence of processing operations, that claim 1 provides the advantage of providing a substantially planar surface over which a photosensitive film used for said patterning, may be formed. When the photoresist layer is formed over a planar surface, the photoresist layer is formed to include a uniform thickness and to avoid the necking that otherwise takes place when the photoresist is thinned or absent over high or abrupt steps in the device beneath the photoresist. (Applicants point out that photoresist is formed by a coating and spinning photoresist.

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process that forms a smooth and level upper photoresist surface. As such, the photoresist layer will be thin or missing in areas over high or abrupt steps.)

As conceded by the Examiner in paragraph 3, Clark does not disclose this limitation. Neither does Inaba. Inaba does not teach planarizing *prior to* patterning the gate electrode material. The Office action identifies col. 13, ll. 3-37 of Inaba. In this section, Inaba recites: "A polysilicon film is buried in the gate electrode forming mask and the excess polysilicon film is polished by CMP to form the gate electrode 54," col. 13, ll. 13-16. Inaba clearly does not teach "*first planarizing, then patterning*" as in claim 1. Moreover, Clark provides a divot – the central area of projection 51A shown in FIG. 1. Moreover, Clark provides a divot – the central area of projection 51A shown in FIG. 14, to alleviate the step height problem solved by the claimed sequence of first planarizing and then patterning.

Independent claim 1 as well as claims 3-5, 9 and 14-15 which depend from claim 1, are therefore distinguished from the references of Clark in view of Inaba and the rejection of claims 1, 3-5, 9 and 14-15 under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Inaba, should be withdrawn.

Dependent claim 18, but not its base claim – claim 17, was rejected under this section. Claim 18 is distinguished from the references of Clark and Inaba by virtue of its dependency from claim 17, which is distinguished from Clark in view of Inaba and Kinsbron, et al. (USPN 4,432,132), hereinafter "Kinsbron," for reasons set forth infra with respect to the rejection of claim 17.

II. Rejection of Claims 2, 6-8 and 16-17

In paragraph 4 of the subject Office action, claims 2, 6-8 and 16-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Inaba as applied to claims 1 and 17, and further in view of Kinsbron. Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

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Claims 2, 6-8 and 16 depend from claim 1 and are distinguished from Clark in view of Inaba for reasons set forth above in the discussion of claim 1. Kinsbron has apparently been relied upon for providing a photoresist mask of substantially uniform thickness on a planar top surface of gate electrode material. Kinsbron does not, however, provide a photoresist mask of substantially uniform thickness over the planarized top surface of a gate electrode material that extends over a semiconductor device as recited in claim 1. Kinsbron merely stands for the proposition, alluded to above, that a photoresist layer has a planar top surface, and when it is applied over a planar surface, the photoresist layer will be of uniform thickness.

Kinsbron therefore does not make up for the above-identified deficiencies of the combination of Clark and Inaba and therefore claims 2, 6-8 and 16 are also distinguished from the references of Clark, Inaba and Kinsbron. The rejection of claims 2, 6-8 and 16 should therefore be withdrawn.

Independent claim 17 recites the features of:

the semiconductor device having a projecting fin;

a multiple gate electrode on each of the opposed sides of the fin, the multiple gate electrode formed of a layer of gate electrode material and having a substantially planar surface disposed atop the gate dielectric film formed over the top of the fin and extending distally past each of the opposed sides of the fin; and

a patterned mask on the planar surface of the multiple gate electrode, the patterned mask having a substantially uniform thickness and a substantially planar surface including over the fin.

As discussed above with respect to claim 1, Clark and Inaba in combination do not teach *first* planarizing the gate electrode material extending over the semiconductor device, *then* patterning the gate electrode material. The combination of Clark and Inaba therefore cannot teach the distinguishing feature claimed in claim 17, namely, having a patterned mask with uniform thickness and a substantially planar top surface formed

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over the planar surface of the multiple gate electrode disposed over the fin. Claim 17 is therefore distinguished from Clark in view of Inaba. Kinsbron simply provides a photoresist mask coating with a planar top surface. As above, the photoresist of Kinsbron only has a uniform thickness when over a planar surface, e.g., see FIGS. 7 and 8 of Kinsbron. Since Kinsbron does not provide the feature of a planarized gate electrode material formed over a semiconductor device, i.e., a fin, prior to patterning, Kinsbron does not make up for the detailed deficiencies of Clark and Inaba.

Claim 17 is therefore distinguished from Clark in view of Inaba and Kinsbron. Claim 18 is similarly distinguished by virtue of its dependency (see Section I). The rejection of claim 17 should therefore be withdrawn.

III. Rejection of Claims 10-13

Claims 10-13 were rejected, in paragraph 5 of the Office action, under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Inaba and further in view of Fried, et al. (UPSN 6,657,252), hereinafter "Fried." Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Fried has apparently been relied upon for providing various different types of gate dielectric materials, but Fried does not make up for the above-stated deficiencies of Clark and Inaba. Fried does not provide the claimed feature of the gate electrode material over a thin film of gate dielectric over the fin. Claim 1 is therefore distinguished from Clark in view of Inaba and in view of Fried. Claims 10-13 depend from claim 1 and are therefore similarly distinguished from these references. The rejection of claims 10-13 under 35 U.S.C. § 103(a) should therefore be withdrawn.

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CONCLUSION

Based on the foregoing, each of pending claims 1-18 is in allowable form and the application in condition for allowance, which action is respectfully and expeditiously requested.

The Assistant Commissioner for Patents is hereby authorized to charge any fees necessary to give effect to this filing and to credit any excess payment that may be associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

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